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Inventor Name Search Result

Your Search was:

Last Name = HUISMAN
First Name = LEENDERT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09524254	6931580	150	03/13/2000	RAPID FAIL ANAYSIS OF EMBEDDED OBJECTS	HUISMAN, LEENDERT M.
09682456	6675323	150	09/05/2001	INCREMENTAL FAULT DICTIONARY	HUISMAN, LEENDERT M.
09827425	6721914	150	04/06/2001	DIAGNOSIS OF COMBINATIONAL LOGIC CIRCUIT FAILURES	HUISMAN, LEENDERT M.
09927011	6901542	150	08/09/2001	INTERNAL CACHE FOR ON CHIP TEST DATA STORAGE	HUISMAN, LEENDERT M.
09930355	6671644	150	08/15/2001	USING CLOCK GATING OR SIGNAL GATING TO PARTITION A DEVICE FOR FAULT ISOLATION AND DIAGNOSTIC DATA COLLECTION	HUISMAN, LEENDERT M.
10191212	6880136	150	07/09/2002	METHOD TO DETECT SYSTEMATIC DEFECTS IN VLSI MANUFACTURING	HUISMAN, LEENDERT M.
10604179	6954916	150	06/30/2003	METHODOLOGY FOR FIXING QCRIT AT DESIGN TIMING IMPACT	HUISMAN, LEENDERT M.
10697365	6865501	150	10/30/2003	USING CLOCK GATING OR SIGNAL GATING TO PARTITION A DEVICE FOR FAULT ISOLATION AND DIAGNOSTIC DATA COLLECTION	HUISMAN, LEENDERT M.
10707373	Not Issued	30	12/09/2003	SCAN CHAIN DIAGNOSTICS USING LOGIC PATHS	HUISMAN, LEENDERT M.
10707957	Not Issued	30	01/28/2004	SEGMENTED SCAN CHAINS WITH DYNAMIC RECONFIGURATIONS	HUISMAN, LEENDERT M.
10708380	Not Issued	30	02/27/2004	METHODS AND APPARATUS FOR DEFECT ISOLATION	HUISMAN, LEENDERT M.
10709672	Not Issued	30	05/21/2004	LEARNING BASED LOGIC DIAGNOSIS	HUISMAN, LEENDERT M.
10710642	Not Issued	30	07/27/2004	Designing Scan Chains With Specific Parameter Sensitivities to Identify Process Defects	HUISMAN, LEENDERT M.
10710879	Not Issued	51	08/10/2004	DEFECT DIAGNOSIS FOR SEMICONDUCTOR INTEGRATED CIRCUITS	HUISMAN, LEENDERT M.
10711765	Not	30	10/04/2004	INSPECTION METHODS AND	HUISMAN, LEENDERT

	Issued			STRUCTURES FOR VISUALIZING AND/OR DETECTING SPECIFIC CHIP STRUCTURES	M.
11006274	Not Issued	30	12/07/2004	Using clock gating or signal gating to partition a device for fault isolation and diagnostic data collection	HUISMAN, LEENDERT M.
06862950	4726023	150	05/14/1986	DETERMINATION OF TESTABILITY OF COMBINED LOGIC END MEMORY BY IGNORING MEMORY	HUISMAN, LEENDERT M.
07900706	5297151	250	06/17/1992	ADJUSTABLE WEIGHTED RANDOM TEST PATTERN GENERATOR FOR LOGIC CIRCUITS	HUISMAN, LEENDERT M.
08811605	6519725	150	03/04/1997	DIAGNOSIS OF RAMS USING FUNCTIONAL PATTERNS	HUISMAN, LEENDERT M.
09032567	6170078	150	02/27/1998	FAULT SIMULATION USING DYNAMICALLY ALTERABLE BEHAVIORAL MODELS	HUISMAN, LEENDERT M.
09379772	6785413	150	08/24/1999	RAPID DEFECT ANALYSIS BY PLACEMENT OF TESTER FAIL DATA	HUISMAN, LEENDERT M.
09026286	6125461	150	02/19/1998	METHOD FOR IDENTIFYING LONG PATHS IN INTEGRATED CIRCUITS	HUISMAN, LEENDERT MARINUS

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Last Name = PASTEL
First Name = LEAH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09908925	6566681	150	07/19/2001	APPARATUS FOR ASSISTING BACKSIDE FOCUSED ION BEAM DEVICE MODIFICATION	PASTEL, LEAH M.
09927011	6901542	150	08/09/2001	INTERNAL CACHE FOR ON CHIP TEST DATA STORAGE	PASTEL, LEAH M.
10707373	Not Issued	30	12/09/2003	SCAN CHAIN DIAGNOSTICS USING LOGIC PATHS	PASTEL, LEAH M.
10711765	Not Issued	30	10/04/2004	INSPECTION METHODS AND STRUCTURES FOR VISUALIZING AND/OR DETECTING SPECIFIC CHIP STRUCTURES	PASTEL, LEAH M.
10906590	Not Issued	30	02/25/2005	CANARY DEVICE FOR FAILURE ANALYSIS	PASTEL, LEAH M.
10907787	Not Issued	30	04/15/2005	SENSOR DIFFERENTIATED FAULT ISOLATION	PASTEL, LEAH M.
10665321	Not Issued	95	09/20/2003	METHOD FOR LOCATING IDDQ DEFECTS USING MULTIPLE CONTROLLED COLLAPSE CHIP CONNECTIONS CURRENT MEASUREMENT ON AN AUTOMATIC TESTER	PASTEL, LEAH M. P.
10697365	6865501	150	10/30/2003	USING CLOCK GATING OR SIGNAL GATING TO PARTITION A DEVICE FOR FAULT ISOLATION AND DIAGNOSTIC DATA COLLECTION	PASTEL, LEAH M. PFEIFER
09681917	6677774	150	06/26/2001	METHOD FOR LOCATING IDDQ DEFECTS USING MULTIPLE CONTROLLED COLLAPSE CHIP CONNECTIONS CURRENT MEASUREMENT ON AN AUTOMATIC TESTER	PASTEL, LEAH M.P.
09682456	6675323	150	09/05/2001	INCREMENTAL FAULT DICTIONARY	PASTEL, LEAH M.P.
10191212	6880136	150	07/09/2002	METHOD TO DETECT SYSTEMATIC DEFECTS IN VLSI MANUFACTURING	PASTEL, LEAH M.P.
10707957	Not	30	01/28/2004	SEGMENTED SCAN CHAINS WITH	PASTEL, LEAH M.P.

	Issued			DYNAMIC RECONFIGURATIONS	
10710222	7005874	150	06/28/2004	UTILIZING CLOCK SHIELD AS DEFECT MONITOR	PASTEL, LEAH M.P.
10710640	6998866	150	07/27/2004	CIRCUIT AND METHOD FOR MONITORING DEFECTS	PASTEL, LEAH M.P.
10710642	Not Issued	30	07/27/2004	Designing Scan Chains With Specific Parameter Sensitivities to Identify Process Defects	PASTEL, LEAH M.P.
10710879	Not Issued	51	08/10/2004	DEFECT DIAGNOSIS FOR SEMICONDUCTOR INTEGRATED CIRCUITS	PASTEL, LEAH M.P.
10710940	Not Issued	30	08/13/2004	METHOD FOR DESIGNING AN INTEGRATED CIRCUIT DEFECT MONITOR	PASTEL, LEAH M.P.
10711083	Not Issued	71	08/20/2004	INTEGRATED CARBON NANOTUBE SENSORS	PASTEL, LEAH M.P.
11280008	Not Issued	71	11/16/2005	Utilizing clock shield as defect monitor	PASTEL, LEAH M.P.
10710114	Not Issued	93	06/18/2004	METHOD AND STRUCTURE FOR DEFECT MONITORING OF SEMICONDUCTOR DEVICES USING POWER BUS WIRING GRIDS	PASTEL, LEAH MARIE P.
10604194	7007214	150	06/30/2003	DIAGNOSABLE SCAN CHAIN	PASTEL, LEAH MARIE PFEIFER
11161181	Not Issued	30	10/13/2005	PASSIVE ELECTRICALLY TESTABLE ACCELERATION AND VOLTAGE MEASUREMENT DEVICES	PASTEL, LEAH MARIE PFEIFER

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IDS Information

Content	Mailroom Date	Entry Number	IDS Review	Reviewer

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